Results of Screening and Qualification Testing of COTS PEMs for Space Applications and Lessons Learned in 2004

Alexander Teverovsky, Chris Greenwell /QSS Group, Inc.,
Ashok Sharma /GSFC/NASA,
Nick Virmani /SWALES Associates

Parts, Packaging, and Assembly Technologies Office,
GSFC, Code 562

Outline

- Statistics of screening and qualification testing results.
- Mistakes and problems during testing and electrical measurements.
- What limits temperature of BI testing?
- Effectiveness of CSAM for screening.
- HAST problems.
- Evaluation of wire bonding.
- Suggested changes in the guidelines EEE-INST-002 for COTS PEMs.

Statistics of Screening

- 13 linear and mixed-signal PEMs (> 4400 samples) have been screened using 3T EM and burn-in.
- 9 lots had no failures during initial EM, 3 lots had 1-2 marginal parametric failures.
- 7 lots had no BI failures, 3 lots had 1 to 2 samples with marginal parametric failures (0.4 to 1.6%), and only one lot had 5 (1%) functional failures.
- Most problems with EM were observed at -40 ^{o}C for high precision ADCs and were likely due to moisture condensation.
- 4 out of 7 lots (763 parts total) had CSAM rejects varying from 1.4 to 35%.

- Problems/cost of ADC testing increase exponentially with resolution → most test labs relax the requirements.
- The number of CSAM rejects far exceeds BI failures.
- Are CSAM rejects potential failures?
- Will delaminations develop after solder reflow and environmental stresses on good samples?

Statistics of Qualification Testing

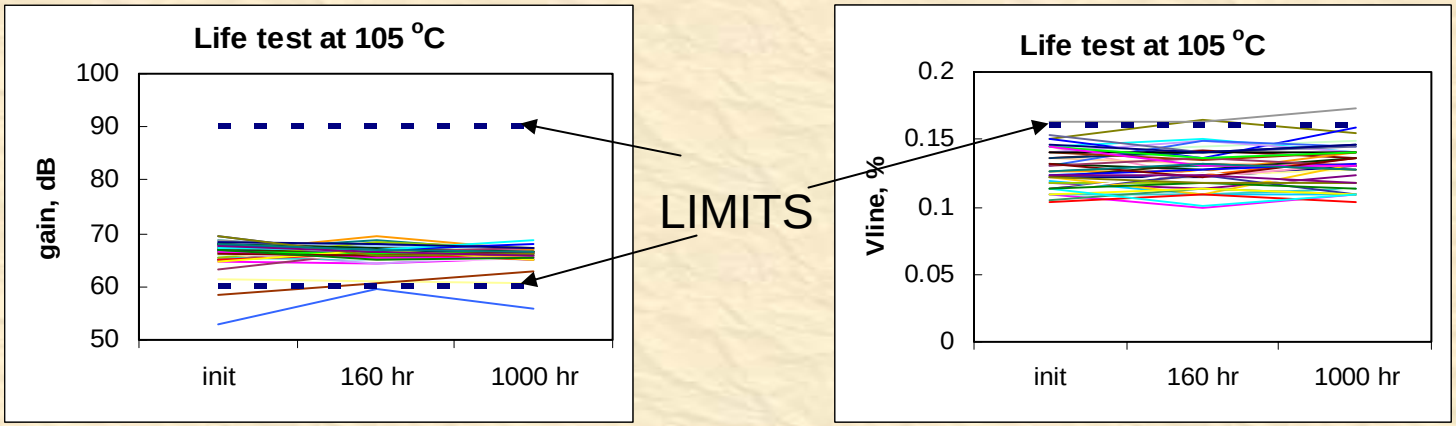
- SMT simulation: 6 out of 10 lots had no failures.
  - 1 out of 32 opamps failed gain marginally;
  - 1 out of 27 comparators failed due to crack/breakdown in PS metallization runs;
  - 8 out of 27 16-bit ADCs failed parametric test marginally.
- HAST: 8 out of 10 lots had no failures.
  - 6 out of 20 12-bit ADCs had marginal failures at -40 ^{o}C;
  - 3/15 step down regulators failed due to EOS and corrosion;
  - 2/12 16-bit ADC failed parametric test marginally.
- HTOL: Only one out of 8 lots had failures.
  - 6/16 16-bit ADC failed parametric test marginally.
- Temperature Cycling: 5 out of 7 lots had no failures.
  - 7/20 12-bit ADC failed parametric test marginally;
  - 1/16 16-bit ADC failed parametric test marginally.

Linear devices are sensitive to mechanical stresses and might fail SMT simulation → more problems with “green” technology?

Qualification: Testing of Unscreened Parts

Currently qualification is performed after screening

- In one of the projects HTOL testing was performed on unscreened parts with interim measurements after 160 hrs.
- Initial parametric failures were allowed to go through the testing to estimate worst-case degradation.



- Marginal parametric failures did not degrade further.
- Qualification testing of COTS PEMs can be performed on unscreened parts.

Test Problems: Human Factor

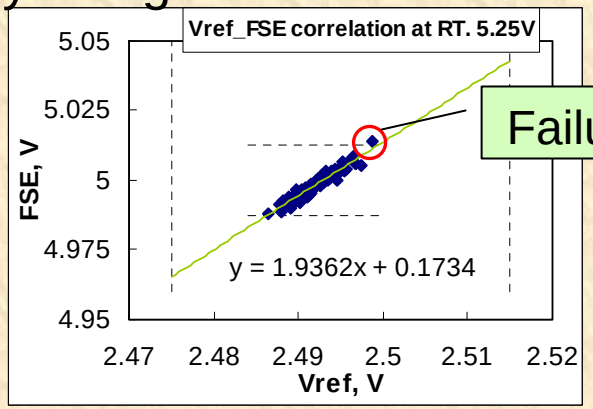
- A wrong set-up was used during BI → multiple failures.
- SMT simulation (preconditioning) was performed before screening → potentially destructive stress.
- A lot, which had BI failures exceeding PDA, was accepted → a problem (wrong BI conditions) was revealed only when one part failed after assembly onto a board.
- A two-side CSAM was performed instead of top side only → the parts were subjected to excessive handling.
- DPA was performed on parts from a non-flight lot.
- DPA was performed not to the existing requirements.
- For AD/DA converters, different test labs use different testing algorithms and criteria → different test results.

Test labs continue making mistakes → additional attention from part engineers is required

Test Problems: Data Sheet

- Example 1, 16-bit ADC
  An average line regulation was 84 uV/V, which substantially exceed the specified value of 0.76 uV/V .
- Example 2, hybrid.
  Data sheet: $T_{op} = T_{st} = 100\ ^oC$.
  This was an error, and per Mfr. Explanation, these temperatures are limited by the encapsulating material: T_{st} = -65 to +150 ^oC, T_{op} = -55 to +150 ^oC (?).
- Example 3, RF devices.
  $T_{jmax} > T_{st}$ because T_{jmax} =Tg?

- Example 4, ADC.
  Inconsistent requirements for FSE and Vref. FSE failure could be eliminated by using external Vref.



Correlation between full scale error and voltage reference measurements (dashed lines are the limits)

Data sheets might have mistakes

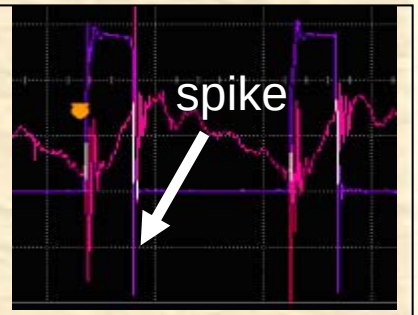
Test Problem: Fixtures and Accessories

Example: Testing of High Power Devices

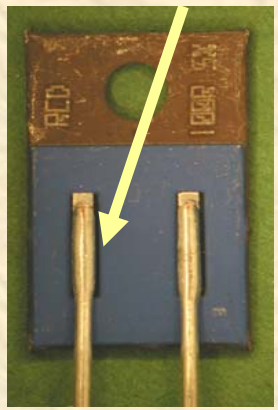
- Inductance of wires and load resistors create voltage spikes
- Some wire-wound resistors have L>10 μH resulting in spikes of >10V and damaging the parts → film resistors were used.
- Two resistors out of ~100 were found to have intermittent contact.
- Several test sockets failed after a few insertions → a new design was required.

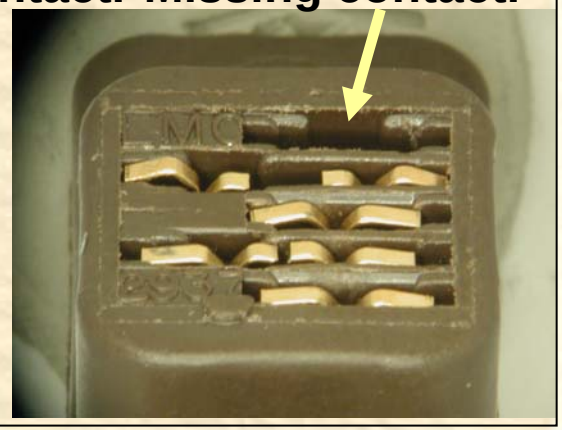
$$V_{SP} = \frac{L}{R} \times \frac{dV}{dt}$$

At dV=30V, dt=0.1μs, R=100 Ohm, and L=10 μH, V_{SP} > 30V



Intermittent contact. **Missing contact.**





A poor reliability of test fixtures and accessories might cause damage to the parts during BI/HTOL testing.

BI Conditions Used

PEM	Package	T_{op}, °C	T_{jmax}, °C	BI T, °C/t, hr
16-bit DAC	SSOP28	85	150	85/336
step-down regulator	PDIP16	85	125	85/336
comparator	SOT23-5	85	150	85/336
current amplifier	SOIC8	125	150	125/168
step-down regulator	MSOP 8	85	125	85/336
quad opamp	14-TSSOP	125	150	125/168
comparator	SO-8	85	150	85/168
16-bit ADC	36-SSOP	85	125	85/168
quad opamp	SO-14	85	150	85/590
12-bit ADC	8-uMAX	85	150	85/168
12-bit DAC	14-QSOP	85	150	85/168
step-down regulator	5-TO220	85	125	105/168

Additional analysis has been performed

- In most cases Top has been chosen as a BI temperature.
- A recommended condition: 85°C/590hr is difficult to impose.
- Is there a risk of exceeding Top and what is the value of reduced-time BI testing?

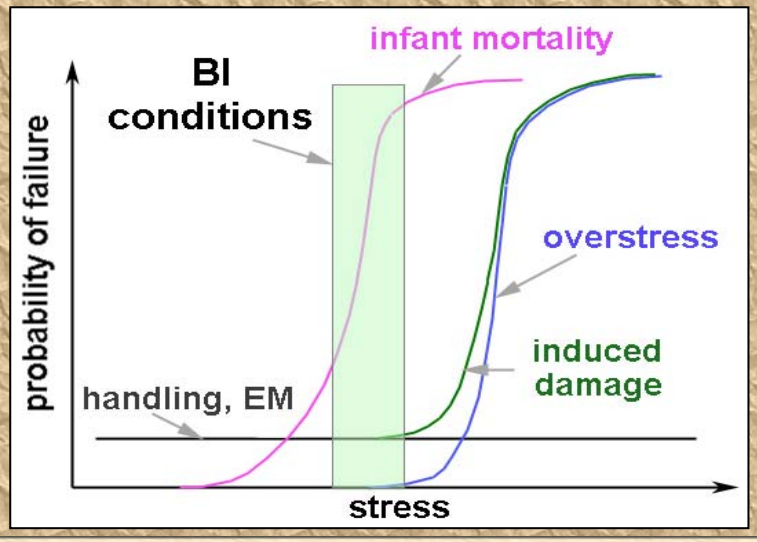
What Limits Testing Temperature?

- Characteristic temperatures for PEMs: T_{op}, T_{jmax}, T_{st}, Tg
- Manufacturers warn that exceeding T_{op}, T_{jmax}, and T_{st} might affect reliability of the part.

- Often P_{max} is used instead of T_{jmax}. $T_j = T_o + P_{max}/\theta_{ja}$. Calculations yield T_{jmax} ~150 ^oC ("gold standard"?). → P_{max} is just a result of reverse calculations.
- Analysis of Mfr.'s data and Tg measurements have shown:
  - 7 out of 11 parts had Tg < T_{jmax};
  - Temperature of life test performed by manufacturers exceeded T_{jmax} in 5 out of 13 cases.

- The significance of the T_{jmax} and T_{st} is not clear.
- Tg does not limit BI/HTOL temperatures.

Problems of Choosing BI Conditions



Example. BI for ADC: 85°C/168hr. Test results. Initial EM: 0/3295; BI: 2 parts failed at RT due to mechanical damage and 1 at -40 °C possibly due to testing.

- BI conditions for military parts (typically 125 °C/160 hrs + bias) were developed and usually performed by manufacturers and have been proven by a long history of testing.
- The risk of exceeding Top during BI can not be eliminated until Top remains in the absolute maximum ratings section of data sheets or the note under AMR is changed.
- For old military parts the risk of inducing defects was not that significant as for advanced PEM.

- Choosing right BI conditions might require additional analysis and testing.
- Reduced-time burn-in testing is not effective due to the possibility of introducing defects by handling and EM.

How Manufacturers Can Exceed T_{jmax} during Life Testing?

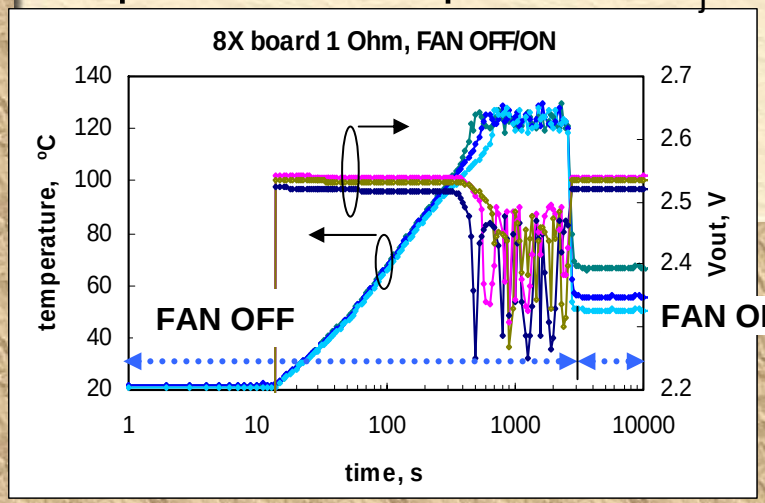
Possible answers:

I. T_{jmax} is not what we think it is.

II. A margin exists between the real T_{jmax} and the data sheet specification.

III. Relaxed electrical biasing conditions.

Example: power step-down regulator with T_{jmax} = +125 °C.
Experiments have shown that the part can not operate at T_j > 125 °C

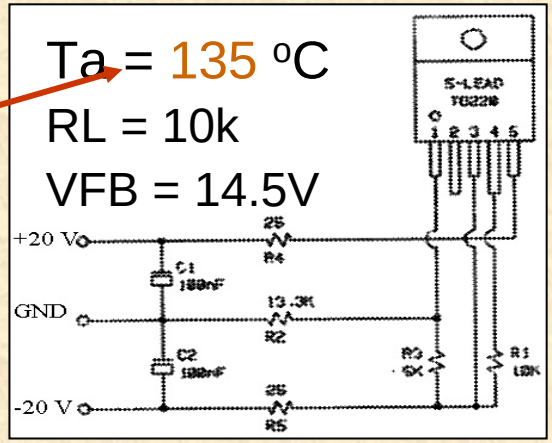


Life test conditions used by manufacturer

Ta = 135 °C

RL = 10k

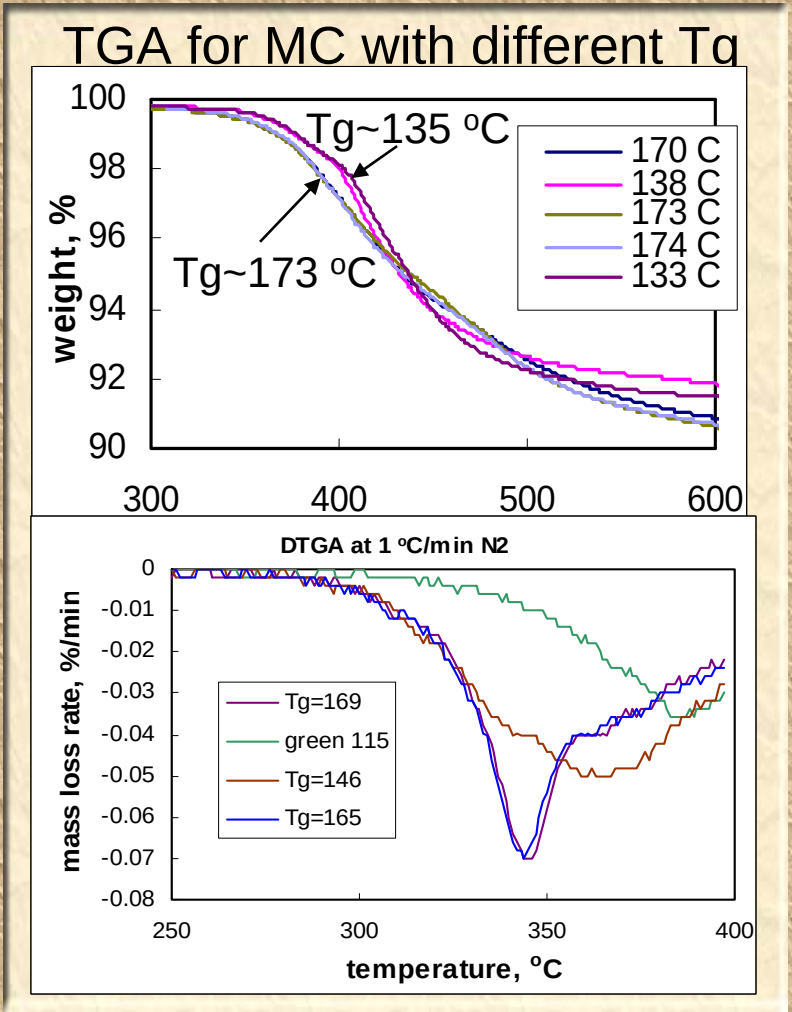
VFB = 14.5V



At these conditions the part does not oscillate and output transistors are not stressed

Manufacturers might perform life testing at non-operational conditions. This limits the value of testing for reliability evaluation.

Does Low Tg Indicate Poor Thermal Stability?

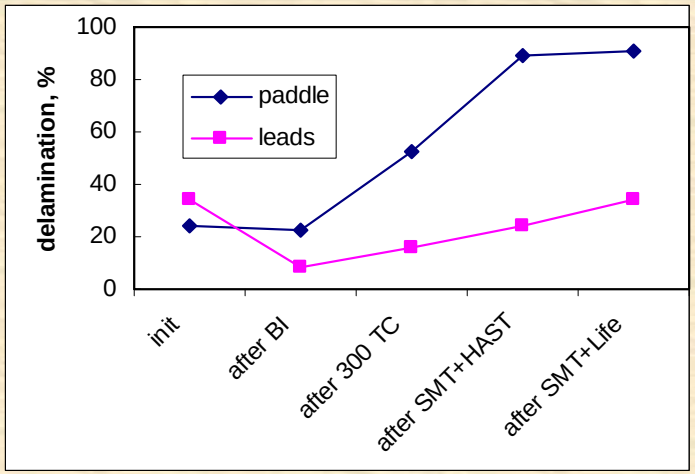


- TGA measurements showed that materials with Tg ~135 °C had better thermal stability compared to MC with Tg~173 °C.
- A green MC with a low Tg of ~115 °C was most thermally stable.

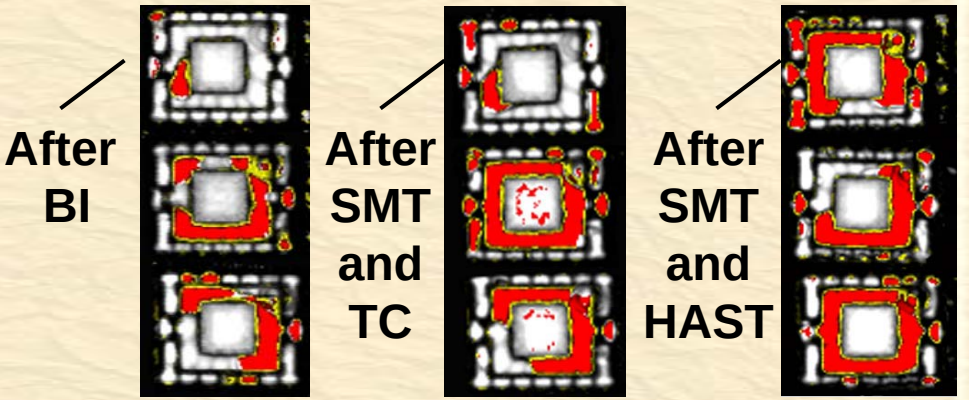
- In general, Tg, is not an indicator of thermal stability of molding compounds.
- Low-Tg MCs are not inferior compared to high-Tg.

C-SAM Examination: TSSOP-14 - style Packages

- Screening: no electrical failures in 245 parts; however, 105 devices failed CSAM examination.
- Testing: 20 worst-case CSAM rejects were subjected to HAST and 300 TC from -65 to +150 ºC. → No failures.



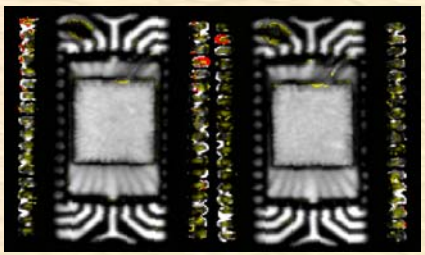
Evolution of delaminations



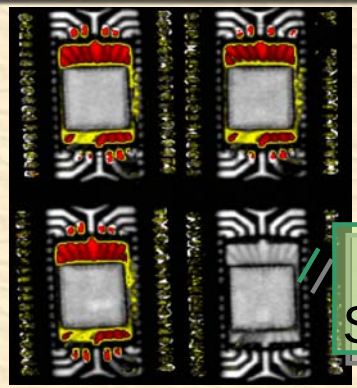
- Delaminations are changing after ES and SMT simulation → CSAM as a screening procedure is not effective.
- Delaminations at paddle and secondary wire bonds did not cause failures.

C-SAM Examination: SSOP-36 - style Packages

- Screening: no delaminations in 123 devices observed during CSAM examination.
- Qualification testing: most parts had paddle and finger-tip delaminations after SMT simulation.



Screening



After HTOL and TC

After HAST

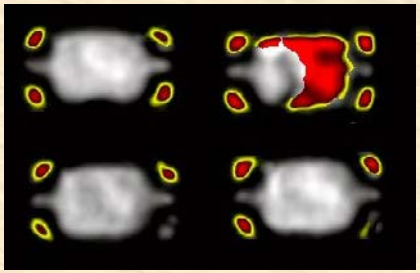
Delaminations are mostly introduced during SMT simulation

→ CSAM is not effective as a screening procedure.

C-SAM Examination: SOT-223 - style Packages

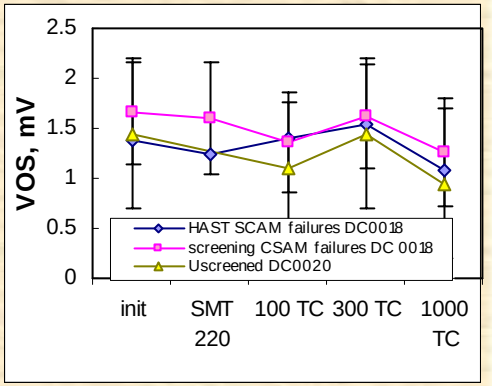
- CSAM failures during screening: 15/79; after HAST: 14/14.
- No electrical failures during screening and qualification.

Delaminations at secondary WB



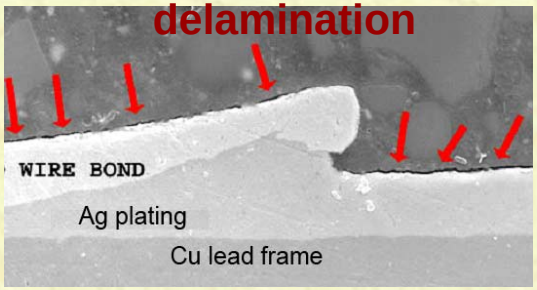
To evaluate the risk related to delaminations, three groups of parts were subjected to preconditioning per JESD22-A113 and 1000 TC from -55 to 125 °C.

Effect of TC on VOS



No failures and/or substantial parametric changes during testing

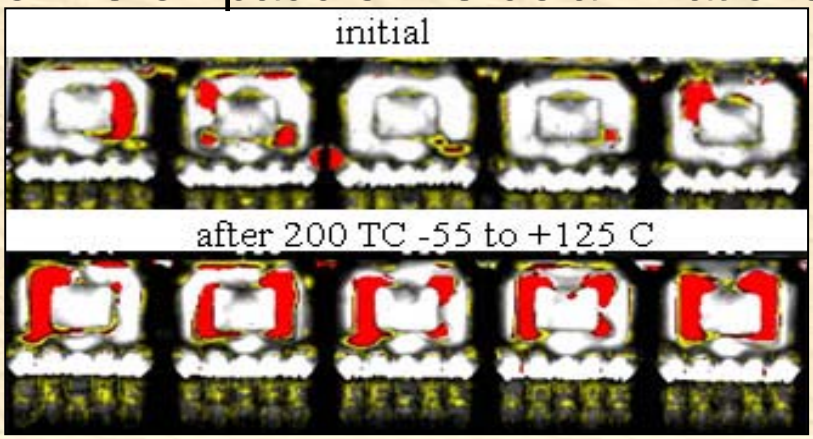
- Delaminations at Au/Ag bonds are common defects in PEMs.
- Secondary bonds are strong enough to provide reliable connection even in the presence of delaminations.



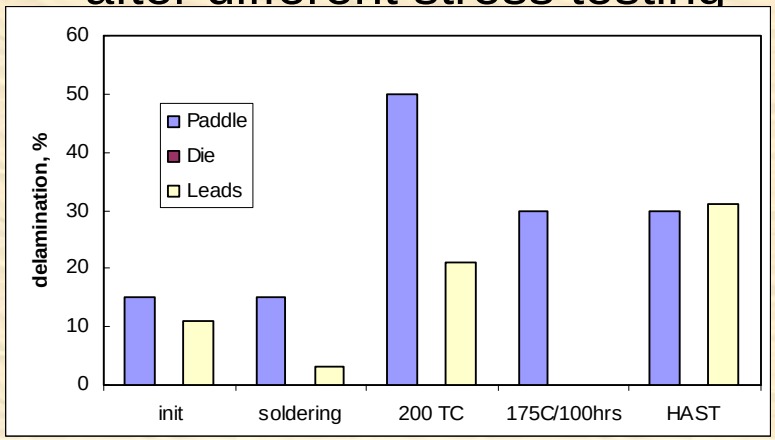
C-SAM Examination: TO220-style Packages

CSAM for screening was optional based on results of qualification testing

Evolution of CSAM images: effect of TC on paddle-MC delaminations



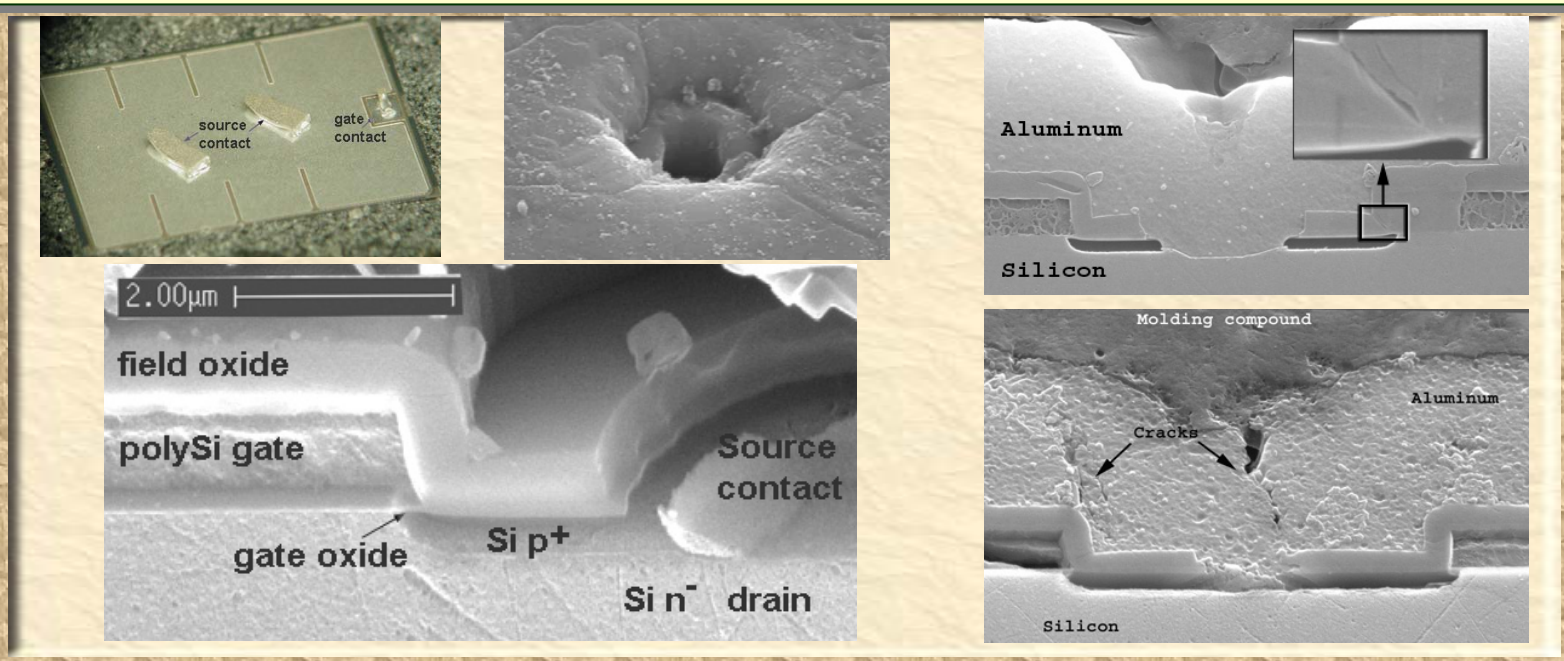
Proportion of delaminations after different stress testing



- No delaminations in the most critical, top-of-die areas.
- Delaminations at paddle and leads (at secondary WB) increase after environmental stress testing.
- No failures during reliability testing of delaminated samples.
- There is no need for using CSAM as a screening procedure.

Follow-up Investigation: Moisture-Induced Charge Instability in HEXFETs

Analysis of HEXFET failures after HAST showed that the failures were due to moisture-induced charge instability [IMAPS'04].

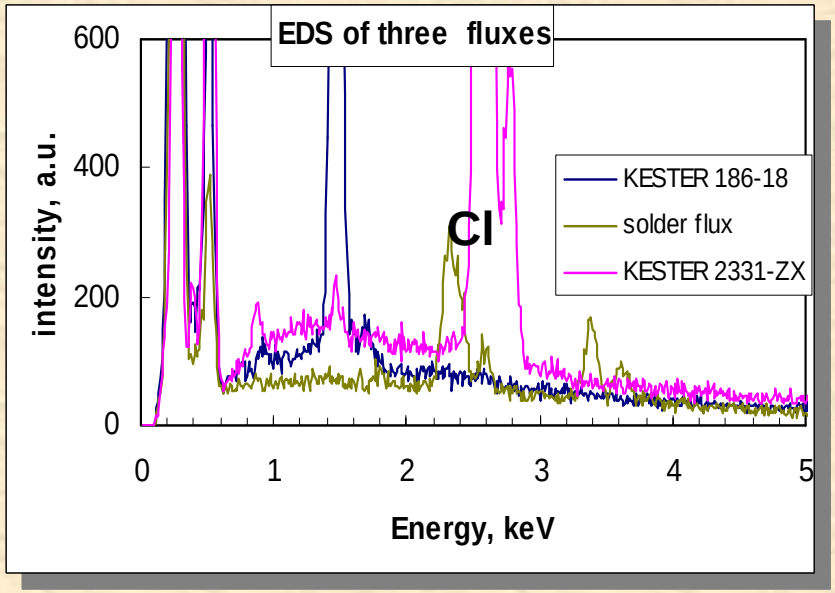


- Water molecules and ions can penetrate to the gate oxide through cracks and pores in Al metallization and SiO_2 layers.
- Nitride passivation is a prime barrier against moisture and ionic contaminations.

Follow-up Investigation: Flux Application During Preconditioning

JEDEC Requirements for Preconditioning and Reproducibility of HAST

- A variety of fluxes used for preconditioning makes them an uncontrollable source of contamination and might cause poor reproducibility of HAST.
- Water-soluble fluxes applied per JESD22-A113D are the most aggressive fluxes and might contain large quantity of contaminations.



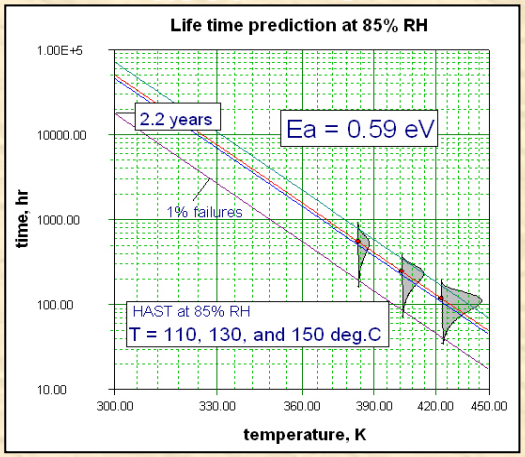
- Activated fluxes are much more aggressive than RMAs, which are typically used for high-reliability applications.

Preconditioning per JESD22-A113D regarding flux application is inadequate to hi-rel parts assembly conditions and might result in failures, which would never occur in real applications.

Follow-up Investigation: HAST Failures in Opamps

Analysis of HAST failures in opamps showed that unbiased HAST might not reveal failures observed during biased HAST [16th M&A COTS 2004].

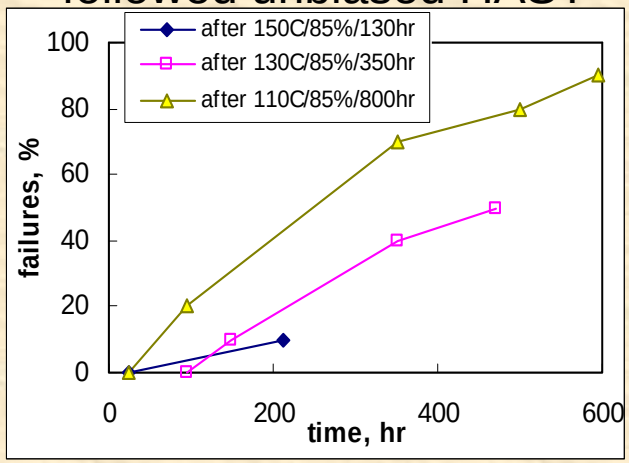
Arrhenius-Weibull model.
Biased HAST.



A relatively low Ea (Peck-Hallberg model Ea ~ 0.79 -1.1 eV) increases the probability of failures at low T

No failures during unbiased HAST even at 150°C/85%

Failures during RT testing followed unbiased HAST



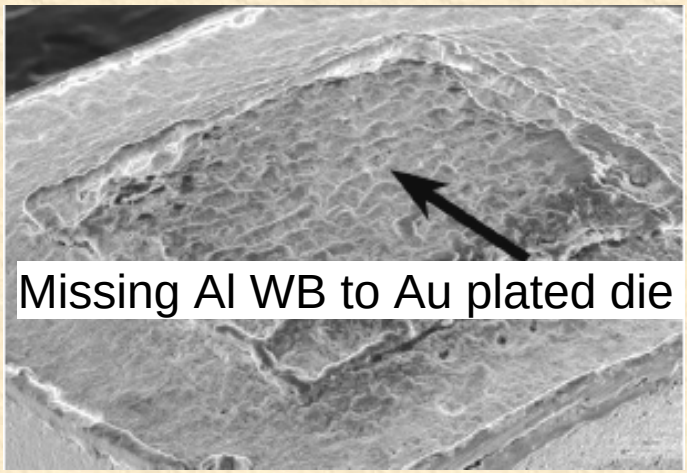
Post-HAST testing at RT under bias causes failures similar to biased HAST

A combination of unbiased HAST with RT bias testing might be a good alternative to biased HAST for QA of parts intended for space applications.

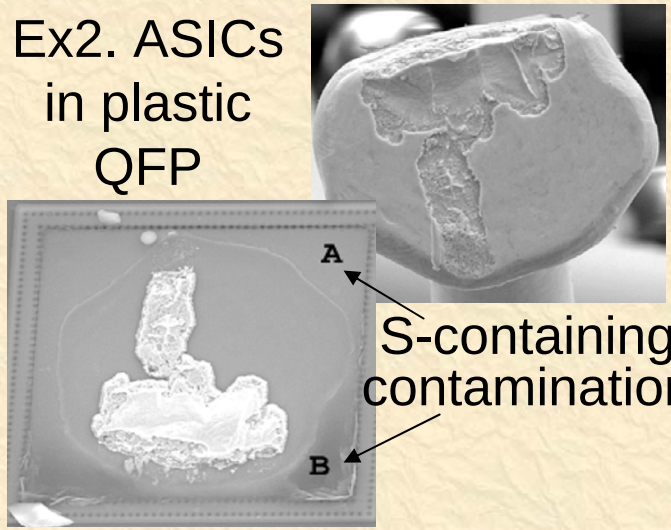
Wire Bond Problems

- Poor quality bonds might pass initial wire pull test.
- Degradation and failures in such WBs might happen with time even at relatively benign storage conditions.

Ex1. Hybrid in plastic package



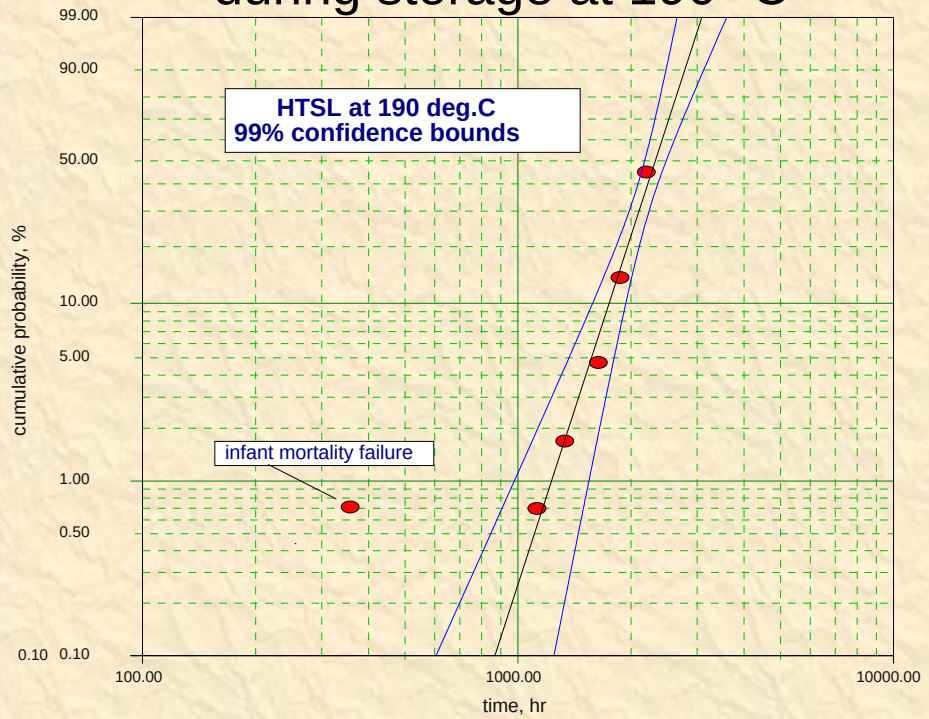
Ex2. ASICs in plastic QFP



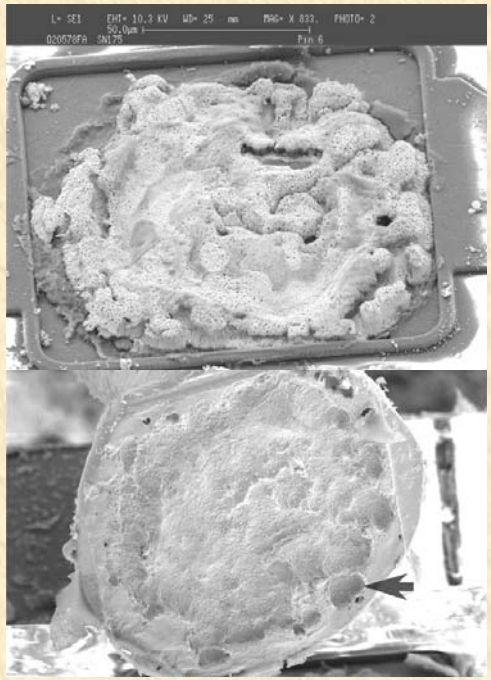
- Substantial portion of reliability issues are now at the packaging level.
- How to evaluate quality and reliability of wire bonds in PEMs?

Evaluation of WB Quality

Weibull distribution of WB Rc failures during storage at 190 °C



Examples of WB failures after HAST



- A technique for WB reliability evaluation is currently under development at the GSFC PA Lab.
- This technique is non-destructive and does not require full electrical characterization of the part.

Suggestions for Changes in PEM Guidelines

- **General**
  - Reinforce engineering control over planning and implementation of S&Q to avoid mistakes.
- **Screening**
  - Make CSAM examinations optional based on results obtained during qualification testing.
  - Remove warning about Tg as a limiting factor during burn-in testing.
- **Qualification**
  - Allow qualification testing of non-screened devices, provided larger quantity is used and interim measurements are performed during life testing to simulate BI conditions.
  - Replace unbiased HAST with a moisture-resistance test, MRT, (a combination of unbiased HAST and biased testing).

Suggestions for Changes in PEM Guidelines (cont.)

- **Qualification, (cont.)**
  - Eliminate flux application during preconditioning per JEDEC standard JESD22-A113-B. Add environmental contamination testing: MRT after SMT simulation followed by application of a specified activated flux.
  - In cases when DPA indicates problems with intermetallic formation at wire bonds (even when wire pull results are acceptable), perform a wire bond qualification testing.
- **DPA**
  - The proportion of area where intermetallics at Au/Al wire bond are formed should be evaluated. A 50 % criteria for bond area with intermetallic formed might be used to discriminate adequate and poor quality wire bonds.